REMARKS

Reconsideration of this application, as amended, is respectfully requested. The following remarks are responsive to the Office Action mailed January 9, 2004.

Double Patenting

Claims 18-30 are provisionally rejected under the doctrine of obviousness-type double patenting as being unpatentable over claims 21-40 of copending Application No. 09/023,170 and claims 15-31 of copending Application No. 09/023,172. Therefore, a terminal disclaimer regarding claims 18-30, as presently amended, is filed herewith.

Claim Objections

Claim 18 is objected to because of the second occurrence of the word "of" in the claim. Accordingly, the above-identified use of the word "of" has been removed from claim 18 as amended.

Claim 21 is objected to because of the second occurrence of the word "a" in the claim. Accordingly, the above-identified use of the word "a" has been removed from claim 18 as amended.

Claim Rejections

Claims 18-21, 23, 24, 27, and 30 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 4,045,781 (hereinafter "Levy").

Claim 18 as presently amended to more clearly claim that the memory module controller serves as a **direct** interface to the system memory controller. Levy, on the other hand, teaches using an associative memory between the memory management unit and the memory control and timing/memory tranceiver units (figure 1). Indeed, Levy teaches a data processing system that provides for overlapping data transfers without the need for multiple control pins (Col. 3, Lns. 57-61) using an associative memory to control asynchronous transfers from or to a location in other down-stream memory modules (Col. 4, Lns. 20-25).

Although the added limitation of a "direct" interface is intended to more clearly point out one aspect of Applicant's invention, it is not added to merely avoid the teachings of Levy. Applicant asserts that Levy does not teach interfacing a system memory controller to a memory management unit, but rather teaches using an intermediate associative memory to interface a memory management unit to the memory control and timing/memory tranceiver combination. Furthermore, Applicant does not, in adding the limitation to claim 1 mentioned above, intend to limit the invention from using other interface logic coupled to the memory module controller unit to facilitate the communication between the system memory controller and the memory module controller.

Accordingly, it is respectfully asserted by Applicant that presently-amended claim 18 is not anticipated by Levy and is in condition for allowance.

Claims 22, 25, 26, 28, and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 4,045,781 to Levy et al.

In view of the above amendments and arguments regarding claim 18, it is asserted by Applicant that limitations within claims 22, 25, 26, 28, and 29 are not taught or suggested by Levy, and are therefore not obvious in view of Levy. Accordingly, Applicant respectfully asserts that claims 22, 25, 26, 28, and 29 are in condition for allowance.

Please charge any additional fees to our Deposit Account No. 02-2666.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Date: March 12, 2004

John Patrick Ward
Reg. No. 40,216

12400 Wilshire Blvd.
Seventh Floor
Los Angeles, CA 90025-1030
(408) 720-8300